In the Office Action, claims 1, 2, and 4-9 were allowed by the Examiner. Claims 27-31 and 33-34 were rejected under 35 U.S.C. § 102(b) as allegedly being anticipated by Yamaguchi, et al (U.S. Patent No. 5,144,393). The Examiner's rejections are respectfully traversed.

With regard to independent claim 27, Applicants describe and claim a transistor. The transistor includes a substrate, a gate insulation layer formed above said substrate, and a gate electrode formed above said gate insulation layer. The gate electrode includes an upper portion comprised of polysilicon and a lower portion. The upper portion has a plurality of extensions formed thereon, which extend laterally beyond the lower portion of the gate electrode by an amount that decreases from bottom to top of the upper portion.

As understood by the undersigned, Yamaguchi is directed to a polysilicon source-drain (PSD) transistor. In particular, the PSD transistor described by Yamaguchi includes a T-shaped gate electrode formed of polycrystalline silicon. See, *e.g.* Yamaguchi, col. 2, ll. 7-11 and Figure 7. However, as admitted by the Examiner at item 8 on page 5 of the previous Office Action mailed on May 8, 2002, Yamaguchi does not expressly disclose a plurality of extensions that decrease from bottom to top of the upper portion. Thus, Applicants respectfully submit that independent claim 27, and claims 28-31 and 33-34 depending therefrom, are not anticipated by Yamaguchi and request that the Examiner's rejections of these claims under 35 U.S.C. § 102(b) be withdrawn.

Moreover, it is respectfully submitted that claims 27-31 and 33-34 are not obvious over Yamaguchi. To establish a *prima facie* case of obviousness, three basic criteria must be met. First, the prior art reference (or references when combined) must teach or suggest all the claim limitations. *In re Royka*, 490 F.2d 981, 180 U.S.P.Q. 580 (CCPA 1974). Second, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally

available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. That is, there must be something in the prior art as a whole to suggest the desirability, and thus the obviousness, of making the combination. *Panduit Corp. v. Dennison Mfg. Co.*, 810 F.2d 1561 (Fed. Cir. 1986). In fact, the absence of a suggestion to combine is dispositive in an obviousness determination. *Gambro Lundia AB v. Baxter Healthcare Corp.*, 110 F.3d 1573 (Fed. Cir. 1997). The mere fact that the prior art can be combined or modified does not make the resultant combination obvious unless the prior art also suggests the desirability of the combination. *In re Mills*, 916 F.2d 680, 16 U.S.P.Q.2d 1430 (Fed. Cir. 1990); M.P.E.P. § 2143.01. Third, there must be a reasonable expectation of success. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 U.S.P.Q.2d 1438 (Fed. Cir. 1991); M.P.E.P. § 2142. A recent Federal Circuit case emphasizes that, in an obviousness situation, the prior art must disclose each and every element of the claimed invention, and that any motivation to combine or modify the prior art must be based upon a suggestion in the prior art. *In re Lee*, 61 U.S.P.Q.2d 143 (Fed. Cir. 2002). Conclusory statements regarding common knowledge and common sense are insufficient to support a finding of obviousness. *Id.* at 1434-35.

As discussed above and acknowledged by the Examiner, Yamaguchi does not describe or suggest an upper portion of a gate electrode having a plurality of extensions that decrease from bottom to top of the upper portion. Moreover, Yamaguchi provides no suggestion or motivation to modify the prior art to arrive at Applicants' claimed invention. In particular, Yamaguchi provides no suggestion or motivation for an upper portion of a gate electrode having a plurality of extensions that decrease from bottom to top of the upper portion.

For the aforementioned reasons, it is respectfully submitted that all claims pending in the present application are in condition for allowance. The Examiner is invited to contact the undersigned at (713) 934-4052 with any questions, comments or suggestions relating to the referenced patent application.

Respectfully submitted,

Date: 1/7/03

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AGENT FOR APPLICANTS

AMENDED CLAIMS FOR SERIAL NO. 09/847,622

27. (Twice Amended) A transistor, comprising:

a substrate;

a gate insulation layer formed above said substrate; and

a gate electrode formed above said gate insulation layer, said gate electrode having an upper portion comprised of polysilicon and a lower portion, said upper portion having a plurality of extensions formed thereon, said extensions of said upper portion extending laterally beyond said lower portion of said gate electrode by an amount that decreases from bottom to top of the upper portion.